Switchmode DC-DC Converter Family Using HIP6006 and HIP6007 PWM Controller ICs

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Introduction

Today's high-performance microprocessors present many challenges to their power source. High power consumption, low bus voltages, and fast load changes are the principal characteristics which have led to the need for a switch-mode DC-DC converter local to the microprocessor. Primarily created to serve this specific applications field, the Intersil HIP6006 and HIP6007 are voltage-mode controllers with many functions needed for implementing high-performance voltage regulators. Figure 1 shows a simple block diagram of the HIP6006 and HIP6007. Each contains a high-performance error amplifier, a high-accuracy reference, a programmable free-running oscillator, and overcurrent protection circuitry. The HIP6006 has two MOSFET drivers for use in synchronous-rectified Buck converters. The HIP6007 omits the lower MOSFET driver for standard Buck configurations. A more complete description of the parts can be found in their data sheets [1, 2].

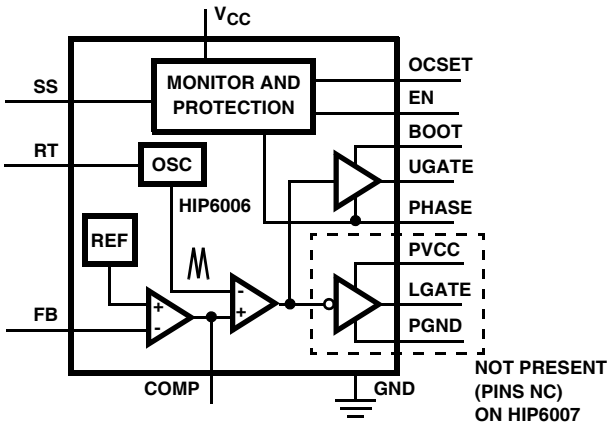


FIGURE 1. BLOCK DIAGRAM OF HIP6006 AND HIP6007

This application note details the HIP6006 and HIP6007 in DC-DC converters for applications requiring a tightly regulated, fixed output voltage. However, high performance microprocessors aren't the only possible applications of this affordable technology. Any low-cost application requiring a DC-DC converter can benefit from one of the designs presented in this application note.

HIP6006/7EVAL1 Reference Designs

The HIP6006/7EVAL1 is an evaluation board which highlights the operation of the HIP6006 or the HIP6007 in an embedded motherboard application. The evaluation board can be configured as either a synchronous Buck (HIP6006EVAL1) or standard Buck (HIP6007EVAL1) converter as described in application note AN9722 [3]. This application note is meant to complement application note AN9722 and expand the range of reference designs offered from 9A, down to 6A and 3A, and up to 12A and 15A in both synchronous and standard buck configurations. This way, a power supply designer can easily modify an existing design to suit almost any particular application. In the circuit configurations described in this application note, the HIP6006/7EVAL1 DC-DC converter demo boards are customized to provide up to 15A of current at a fixed output voltage.

Customization of Reference Designs

The HIP6006EVAL1 and HIP6007EVAL1 reference designs are solutions for Pentium-class microprocessors or other DC circuits with current demands of up to 9A. The evaluation boards can be powered from +5V or +12V and a standard Buck or a synchronous Buck topology may be employed. The designs share much common circuitry and the same printed circuit board; additionally, one basic design is employed to meet many different applications. However, employing one basic design for numerous applications involves some trade-offs. These trade-offs are discussed below, in order to help the user optimize any of the given designs, or even create a custom configuration, for a given set of application requirements. Tables 1 and 2 present reference values for all 10 reference designs (3A through 15A, standard or synchronous Buck configuration) optimized for 5V input operation. The control loop, however, was designed in such a way as to allow for stable operation even with 12V input.

Input Capacitor Selection

The number of input capacitors and their capacitance are usually determined by their maximum RMS current rating. A conservative approach is to determine the converter maximum input RMS current, and assume it would all have to be supplied from the input capacitors. By providing enough capacitors to meet the required RMS current rating, one usually provides enough capacitance for proper power de-coupling. The voltage rating at maximum ambient temperature of the input capacitors should be 1.25 to 1.5 times the maximum input voltage, with very conservative figures approaching 2 times the maximum input voltage. High frequency decoupling (highly recommended) is implemented through the use of ceramic capacitors in parallel with the bulk aluminum capacitor filtering.

TABLE 1. HIP6006 DESIGN RECOMMENDATIONS

COMPONENTS	REF. DESIGN	LOAD CURRENT				
		3A	6A	9A	12A	15A
MOSFETs	Q1 Q2	RFP3055 RFP3055	RFP14N05 RFP14N05	RFP25N05 RFP25N05	RFP70N03 RFP70N03	HUF75345P3 HUF75345P3
SCHOTTKY RECTIFIER	CR2	MBR140P	1N5817	MBR340	1N5820	1N5820
NUMBER OF INPUT CAPS	C1-5	1	2	3	4	5
NUMBER OF OUTPUT CAPS	C6-11	2	3	4	5	6
OUTPUT INDUCTOR	L1	PO559 (T38-52 core, 14T of #22 wire)	PO561 (T44-52 core, 12T of #19 wire)	PO343 (T50-52B core, 10T of #16 wire)	PO563 (T60-52 core, 9Tof #16 wire)	PO565 (T68-52A core, 7T of #16 wire)
OCSET RESISTOR	R6	4.02kΩ	4.99kΩ	3.01kΩ	820Ω	680Ω
CONTROL LOOP COMPENSATION	R5 C14 C15	30.1kΩ 33pF 10nF	20kΩ 33pF 10nF	15kΩ 33pF 10nF	12.1kΩ 33pF 22nF	12.1kΩ 33pF 33nF
JUMPER	JP1	Out	Out	Out	Out	Out

TABLE 2. HIP6007 DESIGN RECOMMENDATIONS

COMPONENTS	REF. DESIGN.	LOAD CURRENT				
		3A	6A	9A	12A	15A
MOSFETs	Q1	RFP3055	RFP14N05	RFP25N05	RFP70N03	HUF75345P3
SCHOTTKY RECTIFIER	CR2 CR3	MBR540 None	MSP835 None	None MBR1535CT	None MBR2535CTL	None MBR2535CTL
NUMBER OF INPUT CAPS	C1-5	1	2	3	4	5
NUMBER OF OUTPUT CAPS	C6-11	2	3	4	5	6
OUTPUT INDUCTOR	L1	PO560 (T38-52 core, 18T of #24 wire)	PO562 (T44-52 core, 16T of #20 wire)	PO345 (T60-52 core, 14T of #17 wire)	PO564 (T68-52A core, 16T of #17 wire)	PO566 (T68-52A core, 17T of #17 wire)
OCSET RESISTOR	R6	4.02kΩ	4.99kΩ	3.01kΩ	820Ω	680Ω
CONTROL LOOP COMPENSATION	R5 C14 C15	49.9kΩ 22pF 10nF	40.2kΩ 22pF 10nF	15kΩ 33pF 10nF	33.2kΩ 33pF 33nF	47kΩ 10pF 10nF
JUMPER	JP1	Out	Out	In	In	In

MOSFET Selection

As a supplement to the datasheets' application information on *MOSFET Selection Considerations*, this section shows graphically that a larger, lower $r_{DS(ON)}$ MOSFET does not always improve converter efficiency. Figure 2 shows that smaller RFP25N05 MOSFETs are more efficient over most of the line and load range than larger RFP45N06 MOSFETs. The RFP25N05 (used on the 9A version of HIP6006/7EVAL1) has a $r_{DS(ON)}$ of 47mΩ (maximum at 25^{o}C) versus 28mΩ for the RFP45N06. In comparison to the RFP25N05, the RFP45N06's gain in switching losses offsets its decreased conduction losses at load currents up to about 7A with a 5V input, and about 9A with a 12V input. This data reinforces the need to consider both switching and conduction losses of the MOSFETs.

Schottky Selection

In a synchronous rectified buck regulator configuration (such as a HIP6006EVAL1), the effect of the Schottky diode is minimal, and for most applications, the diode could be excluded from the circuit. In such circuits, the Schottky diode is only conducting during the switching time of the "free-

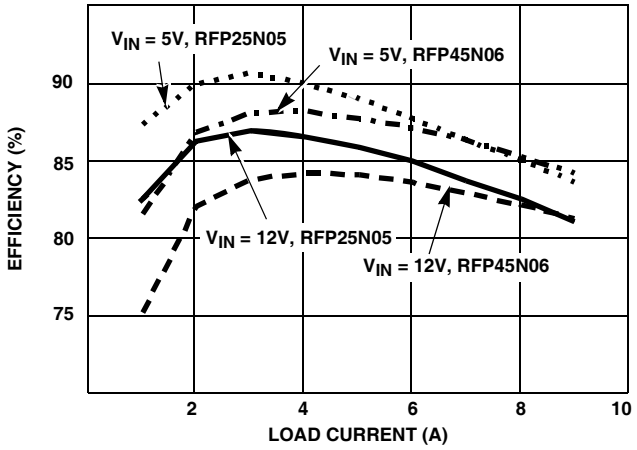


FIGURE 2. HIP6006EVAL1 EFFICIENCY WITH EITHER RFP25N05 OR RFP45N06 MOSFETs

wheeling" MOSFET, basically providing a lower impedance path for the current which otherwise would flow entirely through the body diode of the same MOSFET. This way, reverse recovery and switching losses are reduced to a minimum (providing a good choice for the Schottky selection). Laboratory results have only attributed an efficiency gain of 1 to 2% to the use of an appropriately sized Schottky in a synchronous buck regulator. If absolute peak efficiency warrants the extra cost incurred by the use of an additional semiconductor device, then use a Schottky. If a Schottky is employed, the maximum inductor current should not exceed the absolute peak repetitive forward diode current rating. A low forward conduction voltage drop, along with an average forward current rating equal to at least 20 to 25% of the maximum regulator output current should complete this minimal list of desired requirements.

In the case of a standard buck application (such as the HIP6007EVAL1), however, the requirements are much more stringent. In this case, the free-wheeling inductor current flows entirely through the Schottky diode during the MOSFET's off time. Maximum power dissipated by the Schottky diode can be approximated using the following formula:

$$P_{SCHOTTKY} = (1 - D) \bullet V_F \bullet I_{OUT}, \text{ where}$$

D = regulator duty cycle

I_{OUT} = maximum output current

V_F = Schottky forward conduction drop at I_{OUT}

Effects of the dissipated power on the junction temperature have to be taken into account, and in some cases, the Schottky diode may require heatsinking methods comparable or even exceeding those required by the MOSFET. Selection criteria for the Schottky diode include a repetitive forward current rating exceeding peak inductor current, along with a strong consideration of the thermal parameters of the Schottky package type.

Output Voltage

Simple resistor value changes allow for outputs as low as 1.3V or as high as the input voltage. The steady-state DC output voltage can be set using the following simple formula:

$$V_{OUT} = V_{REF} \bullet \left(1 + \frac{R3}{R2}\right), \text{ where}$$

V_{OUT} = desired DC output voltage of the converter

V_{REF} = HIP6006/7 internal reference voltage (typically 1.27V)

Using the above formula, it can be easily seen that the output voltage of all the reference designs presented in this application note is set for 2.54V.

Output Capacitor Selection

As with the input capacitors, the number of output capacitors is determined by a parameter different than sheer capacitance. Based on the desired output ripple and output transient response, a maximum ESR can be determined. Based on the design's dimensional restraints, an optimum compromise between the number and size of the output capacitors can be reached. Conservative approaches dictate using the data book's maximum values for ESR; this way the design will still meet the initial criteria even at the end of capacitor's active life. High frequency decoupling of the output was not implemented on these designs, since the typical application (microprocessor supply) provides high frequency decoupling components at the load end of the output. In applications requiring good high frequency decoupling, the output should be accordingly decoupled using a few ceramic capacitors. This measure is especially necessary if high ESL output capacitors are used. The following two sections are intended to help select the output capacitors.

Output Ripple Voltage

The amount of ripple voltage on the output of the DC-DC converter varies with input voltage, switching frequency, output inductor, and output capacitors. For a fixed switching frequency and output filter, the voltage ripple increases with the input voltage. The ripple content of the output voltage can be estimated with the following simple equation:

$$\Delta V_{OUT} = \Delta I_L \bullet ESR, \text{ where}$$

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \bullet \frac{V_{OUT}}{V_{IN}} \bullet T}{L_{OUT}}, \text{ and}$$

ESR = equivalent series resistance of output capacitors

V_{IN} = converter input voltage

T = time for one switching cycle (1/f)

L_{OUT} = output inductance

Therefore, for equivalent output ripple performance at V_{IN} = 12V as at 5V, the output filter or switching frequency must change. Assuming 200kHz operation is desired, either the output inductor value should increase or the number of paralleled output capacitors should increase (to decrease the effective ESR).

Output Load Transient Response

At application of a sudden load requiring the converter to supply maximum output current, most of the energy required by the output load is initially delivered from the output capacitors. This is due to the finite amount of time required for the inductor current to slew up to the level of output current required by the load, and results in a temporary dip (ΔV_{LOW}) in the output voltage. At the very edge of the transient, the equivalent series inductance (ESL) of each individual capacitor induces a spike that adds on top of the existing voltage drop due to the equivalent series resistance (ESR). Heavily dependent on the characteristics of the capacitors, as well as the converter and load step parameters, the maximum voltage deviation can occur either at the edges of the load transient ($\Delta V_{EDGELOW}$, $\Delta V_{EDGEHIGH}$), or during the temporary dip/hump in the output voltage. Refer to Figure 3 for illustration of these explanations and the equations to follow. Conversely, at sudden removal of the same output load, the energy stored in the inductor is dumped into the output capacitors, creating a temporary hump (ΔV_{HIGH}) in the output voltage. The amplitude of the two types of voltage transients is different from each other, and a conservative approximation of the components of the output deviation thus incurred can be determined using the following formulae:

$$\Delta V_{EDGELOW} = \Delta V_{EDGEHIGH} = \Delta V_{ESR} + \Delta V_{ESL} \quad \text{(EQ. 1)}$$

$$\Delta V_{LOW} \cong \Delta V_{ESR} + \Delta V_{SAG} \quad \text{(EQ. 2)}$$

$$\Delta V_{HIGH} \cong \Delta V_{ESR} + \Delta V_{HUMP}, \text{ where} \quad \text{(EQ. 3)}$$

$$\Delta V_{ESR} = ESR \bullet I_{TRAN}$$

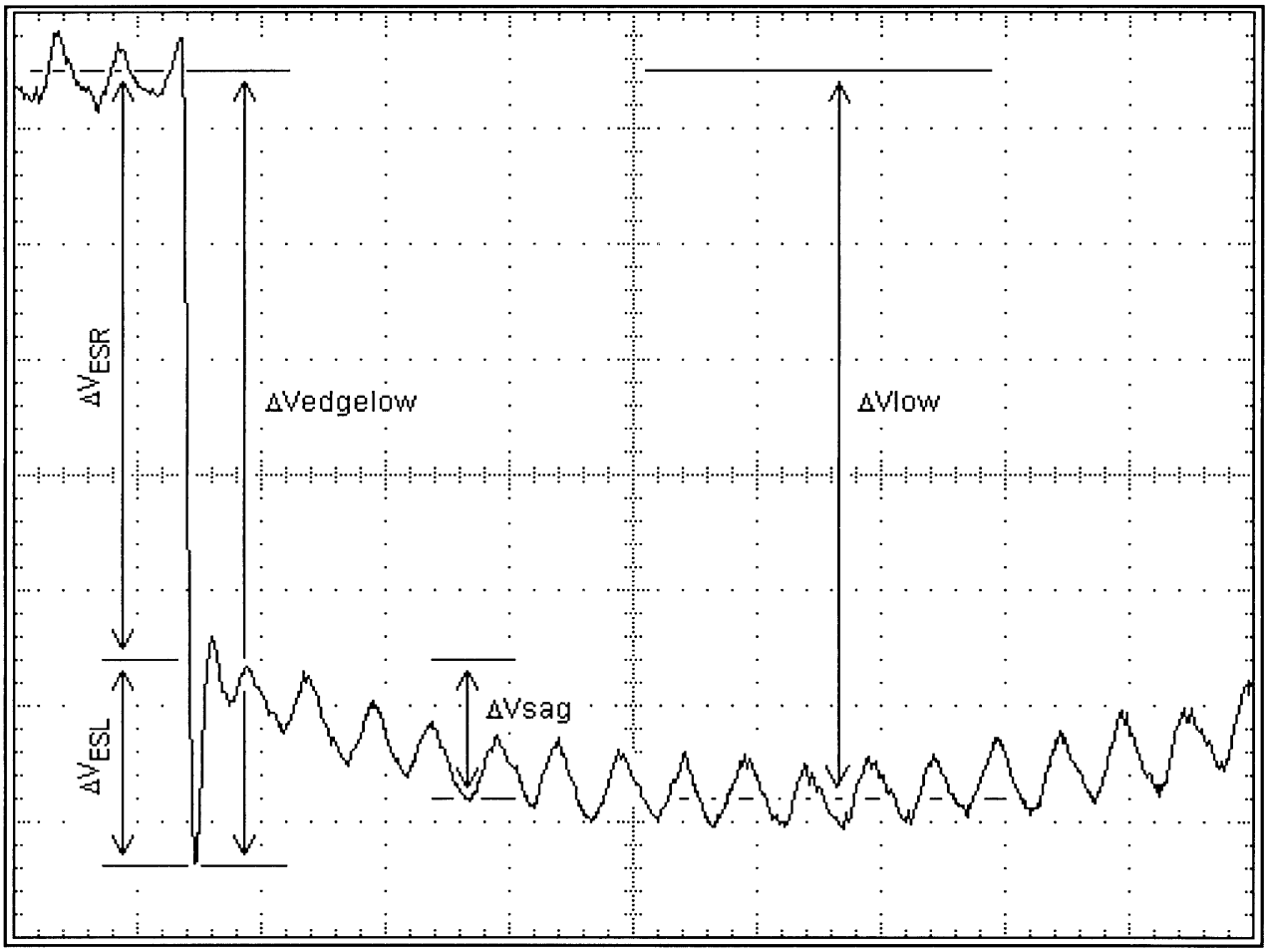


FIGURE 3. TYPICAL CONVERTER OUTPUT VOLTAGE TRANSIENT RESPONSE (LEADING EDGE)

$$\Delta V_{ESL} = ESL \bullet \frac{dI_{TRAN}}{dt}$$

$$\Delta V_{SAG} = \frac{L_{OUT} \bullet I^2_{TRAN}}{C_{OUT} \bullet (V_{IN} - V_{OUT})}$$

$$\Delta V_{HUMP} = \frac{L_{OUT} \bullet I^2_{TRAN}}{C_{OUT} \bullet V_{OUT}}$$, and

I_{TRAN} = output load current transient

C_{OUT} = total output capacitance

Additionally, Equations 1, 2, and 3 are split in two distinct parts: the first part quantifies the effect of the capacitor's ESR on the output voltage and the second part approximates the voltage spike (due to ESL) or droop/hump (due to inductor current slew-up/dump time). These simplified equations assume the inductor will not contribute to the output current until inductor current equals in magnitude the value of the output current.

It can be demonstrated using the above equations that in a typical converter design using aluminum electrolytic capacitors, the ESR is usually far more important than the sheer amount of capacitance offered by the output capacitor bank.

An important parameter mentioned in the above equations is the equivalent series inductance (ESL). Though usually not listed in data books, it can have a serious influence on the quality of the output voltage. Practically, it can be approximately determined if an impedance vs frequency curve is given for a specific capacitor. Thus,

$$ESL \cong \frac{1}{C \bullet (2 \bullet \pi \bullet f_{RES})^2}$$, where

C = capacitor nominal capacitance

F_{RES} =resonant frequency (frequency where lowest impedance is achieved)

ESL has to be taken into account when designing circuits that will supply power to loads with high rate of change, such as microprocessors. For example, when a contemporary microprocessor steps from idle (0.5A) to full operation (10.5A) in 350ns, it creates a rate of change in output current of 30A/µs. Consider the 12A reference design, with an ESL of 2nH (estimated) per each of the 5 paralleled output capacitors. In this design the output voltage excursion due to ESL amounts to 12mV. As mentioned, this excursion voltage is above and beyond the deviation caused by the ESR, manifesting itself in the form of a spike in the output voltage corresponding to the ascending or descending slope of the output current transient. If extremely tight output regulation is required, the above value might represent an important share of the overall output voltage tolerance budget.

Control Loop Bandwidth

Control loop bandwidth ties in tightly with the ability of a PWM controller IC to maintain a tightly regulated output voltage under various dynamic loading conditions. Generally, the higher the bandwidth, the faster the response of the regulator. However, the bandwidth cannot be extended beyond half the regulator's switching frequency. Similarly, phase margin at the crossover frequency should be better than 45 degrees.

Table 3 shows an example of how the control loop characteristics vary with line voltage and topology. The line voltage determines the amount of DC gain, which directly affects the modulator (control-to-output) transfer function. Benefiting from a 15MHz gain-bandwidth product (GBW) error amplifier, the converter loop gain is unaffected by operational amplifier limitations in most of its applications, thus further simplifying the design of the feedback compensation network. The topology (standard buck or synchronous buck) is important because we have chosen to use a larger output inductor for the standard buck (HIP6007) design. This lowers the boundary between continuous conduction mode (ccm) and discontinuous conduction mode (dcm) operation. Dropping into dcm at light loads can have an adverse effect on transient response of the converter. Under steady-state operation, the HIP6006EVAL1 design will not go into dcm because the lower MOSFET conducts current even at light or zero load conditions.

TABLE 3. CONTROL LOOP PARAMETERS FOR 12A REFERENCE DESIGN

PARAMETER	INPUT VOLTAGE	HIP6006 (I_{OUT} = 12A)	HIP6007 (I_{OUT} = 12A)
LOOP BANDWIDTH	5V	17kHz	24kHz
	12V	60kHz	55kHz
PHASE MARGIN	5V	82deg.	77deg.
	12V	80deg.	67deg.

All the circuits presented in this application note are rather conservatively designed. As it can be seen in Table 3, the phase margin is maintained in the 60 to 80 degree range, which provides for excellent stability, while the loop bandwidth tops at 55 to 60kHz with 12V input. Loop bandwidths approaching half the switching frequency can create basis for instability, so 60kHz is a relatively good, very stable design criteria. However, any of these designs could be further optimized, given a fixed set of operating parameters. Refer to the data sheets' application information on Feedback Compensation for a detailed design procedure.

Efficiency

Figures 4 through 7 display the laboratory-measured efficiency of the HIP6006EVAL1 and HIP6007EVAL1 reference designs versus load current, for both 5V and 12V inputs, with 100 linear feet per minute (LFM) of airflow. The

five curves in each figure depict the individual efficiency for each of the five reference designs (levels of output current). For a given output voltage and load, the efficiency is lower at higher input voltages, due primarily to higher MOSFET switching losses.

Conclusion

The HIP6006/7EVAL1 board lends itself to a variety of DC-DC converter designs. Main beneficiaries of these affordable designs are microprocessors with fixed core voltage requirements. The built-in flexibility allows the designer to quickly modify for applications with various custom requirements, the printed circuit board being laid out to accommodate necessary components and operation at currents up to 15A.

References

For Intersil documents available on the web, see http://www.intersil.com.

[1] *HIP6006 Data Sheet*, Intersil Corporation, FN4306.

[2] *HIP6007 Data Sheet*, Intersil Corporation, FN4307.

[3] *AN9722 Application Note*, Intersil Corporation.

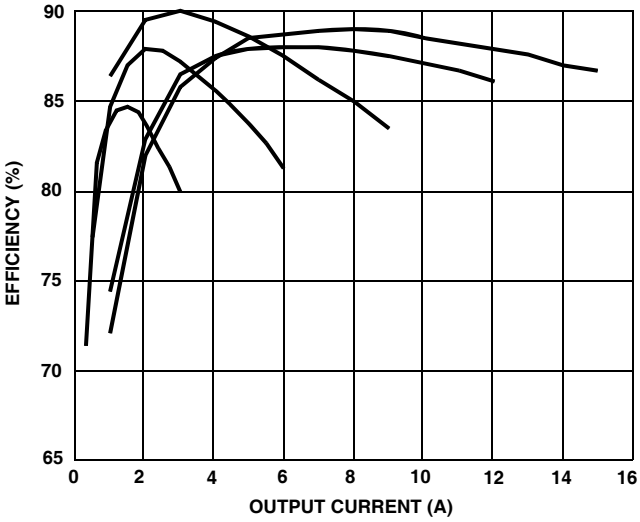


FIGURE 4. HIP6006 REFERENCE DESIGNS AT V_{IN} = 5V

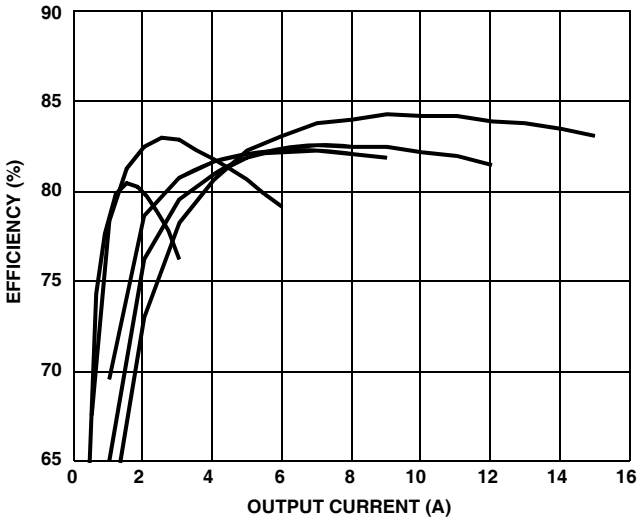


FIGURE 5. HIP6006 REFERENCE DESIGNS AT V_{IN} = 12V

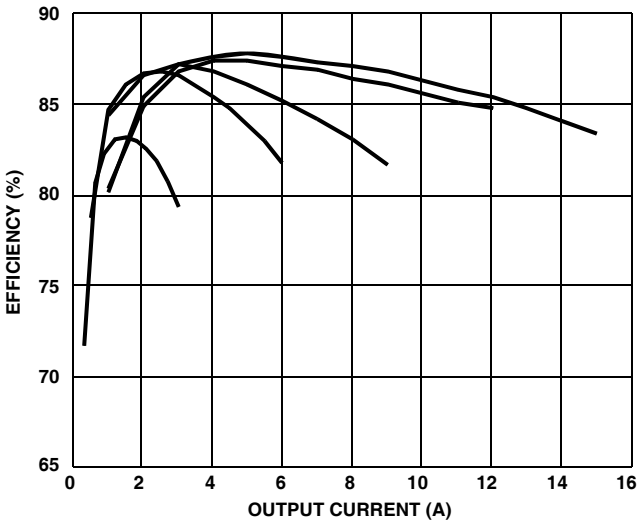


FIGURE 6. HIP6007 REFERENCE DESIGNS AT V_{IN} = 5V

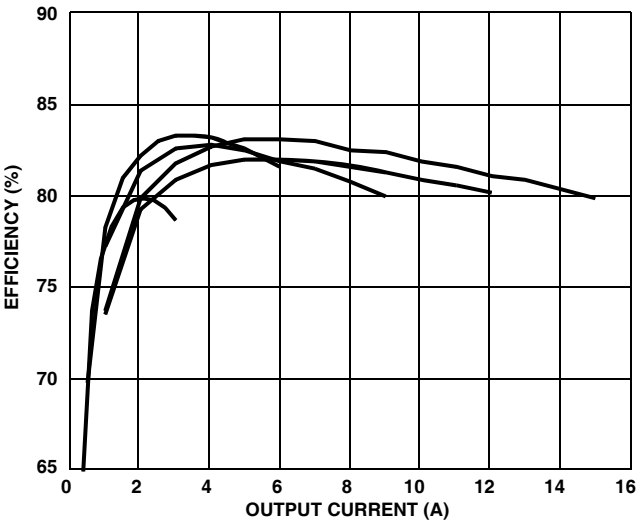
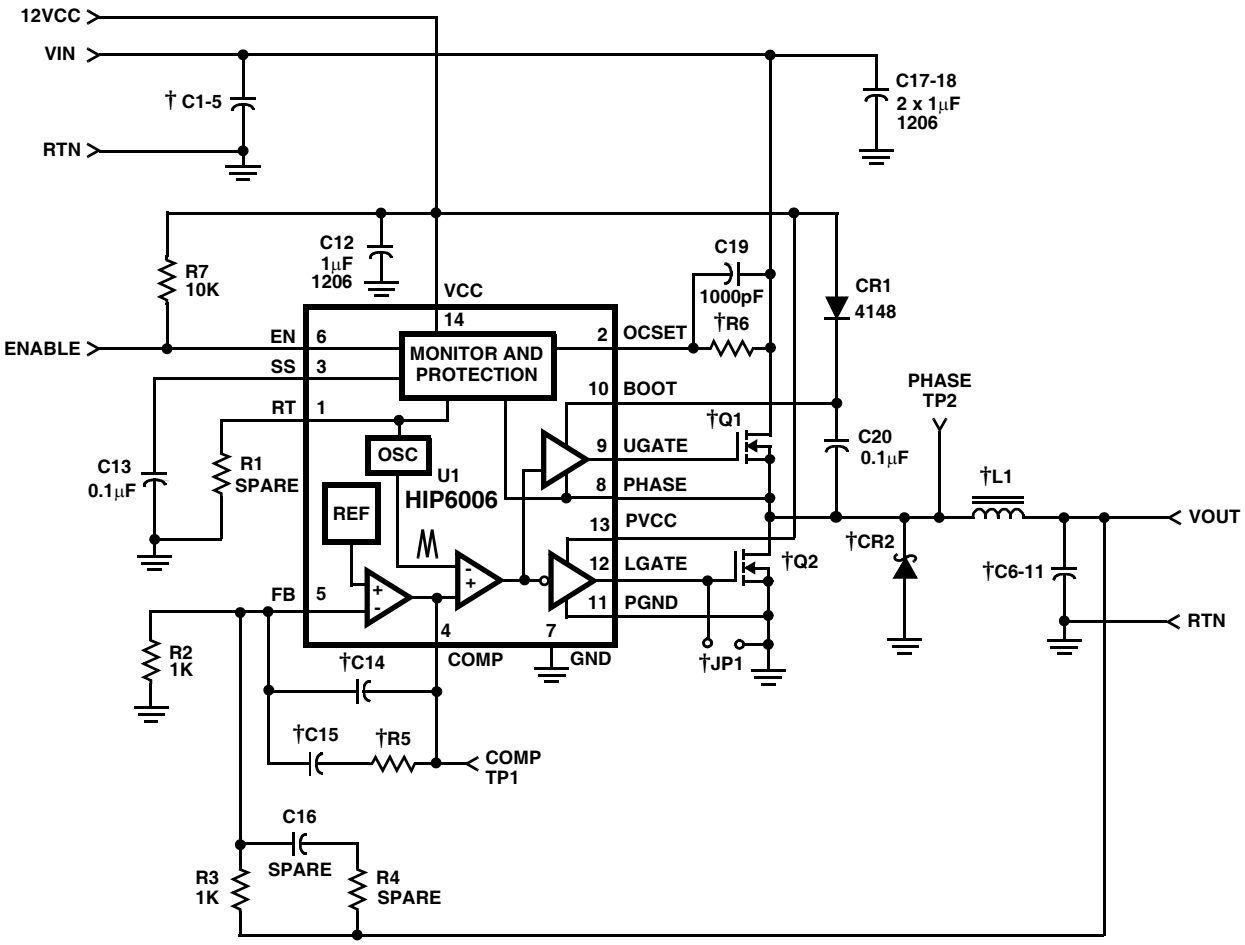


FIGURE 7. HIP6007 REFERENCE DESIGNS AT V_{IN} = 12V

HIP6006EVAL1 Schematic

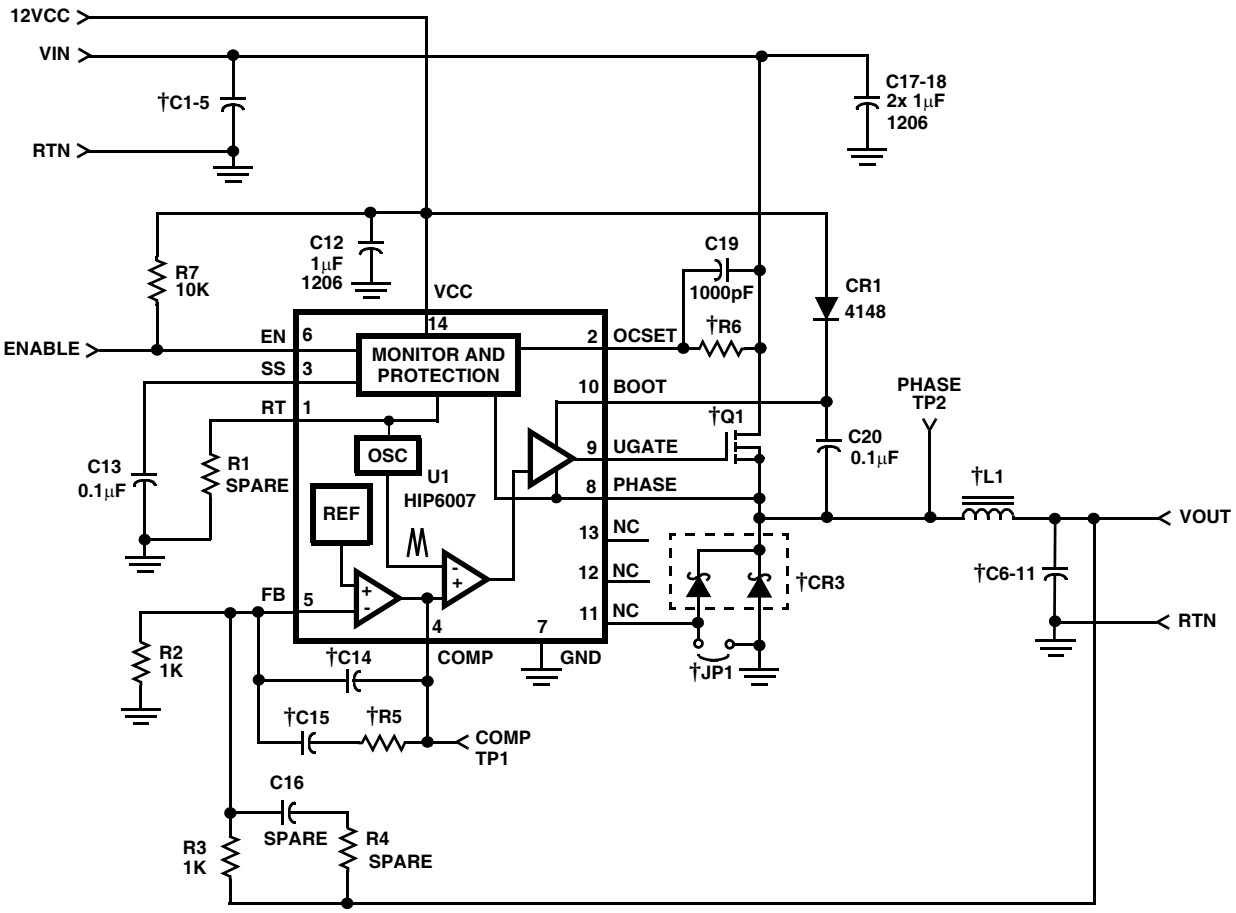


†For more information about these components, please read the application material and consult Table 1.

Bill of Materials for HIP6006EVAL1

PART #	DESCRIPTION	PACKAGE	QTY	REF	VENDOR
25MV680GX	Aluminum Capacitor, 25V, 680µF	Radial 10x22	See Table 1	C1 - C5	Sanyo
6MV1000GX	Aluminum Capacitor, 6.3V, 1000µF	Radial 8x20	See Table 1	C6 - C11	Sanyo
1206YZ105MAT1A	Ceramic Capacitor, X7S, 16V, 1.0µF	1206	3	C12, C17-C18	AVX
1000pF Ceramic	Ceramic Capacitor, X7R, 25V	0805	1	C19	Various
0.1µF Ceramic	Ceramic Capacitor, X7R, 25V	0805	2	C13, C20	AVX/Panasonic
See Table 1	Ceramic Capacitor, X7R, 25V	0805	1	C15	Various
See Table 1	Ceramic Capacitor, X7R, 25V	0805	1	C14	Various
1N4148	Rectifier,100mA, 75V	DO35	1	CR1	Various
See Table 1	Schottky Rectifier	Axial	1	CR2	Motorola
See Table 1	Inductor	Wound Toroid	1	L1	Coiltronics Pulse
See Table 1	MOSFET	TO-220	2	Q1, Q2	Intersil
HIP6006	Synchronous Rectified Buck Controller	SOIC-14	1	U1	Intersil
10kΩ	Resistor, 5%, 0.1W	0805	1	R7	Various
See Table 1	Resistor, 5%, 0.1W	0805		R1	Various
See Table 1	Resistor, 5%, 0.1W	0805	1	R5	Various
1kΩ	Resistor, 5%, 0.1W	0805	2	R2-R3	Various
See Table 1	Resistor, 1%, 0.1W	0805	1	R6	Various
576802B00000	Clip-on Heatsink, TO-220		2		AAVID
1514-2	Terminal Post		6	VIN, 12VCC, VOUT, RTN	Keystone
1314353-00	Test Point, Scope Probe		1	VOUT	Tektronics
SPCJ-123-01	Test Point		3	ENABLE, TP1, TP2	Jolo

HIP6007EVAL1 Schematic

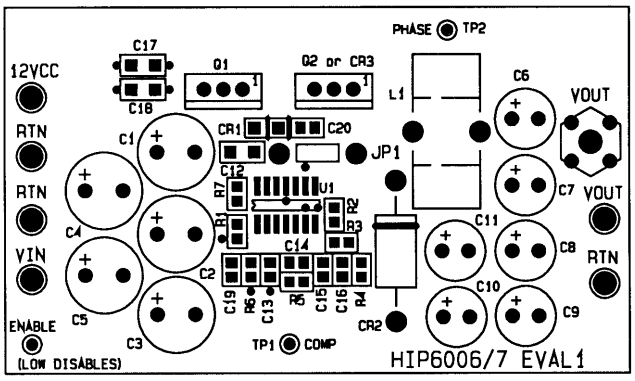


†For more information about these components, please read the application material and consult Table 2.

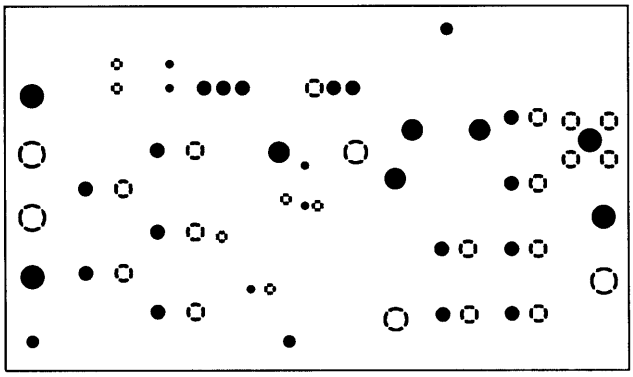
Bill of Materials for HIP6007EVAL1

PART #	DESCRIPTION	PACKAGE	QTY	REF	VENDOR
25MV680GX	Aluminum Capacitor, 25V, 680µF	Radial 10x22	See Table 2	C1 - C5	Sanyo
6MV1000GX	Aluminum Capacitor, 6.3V, 1000µF	Radial 8x20	See Table 2	C6 - C11	Sanyo
1206YZ105MAT1A	Ceramic Capacitor, X7S, 16V, 1.0µF	1206	3	C12, C17-C18	AVX
1000pF Ceramic	Ceramic Capacitor, X7R, 25V	0805	1	C19	Various
0.1µF Ceramic	Ceramic Capacitor, X7R, 25V	0805	2	C13, C20	AVX/Panasonic
See Table 2	Ceramic Capacitor, X7R, 25V	0805	1	C15	Various
See Table 2	Ceramic Capacitor, X7R	0805	1	C14	Various
1N4148	Rectifier, 75V, 100 mA	DO35	1	CR1	Various
See Table 2	Schottky Rectifier	TO-220	1	CR3	Motorola
See Table 2	Inductor	Wound Toroid	1	L1	Coiltronics Pulse
See Table 2	MOSFET	TO-220	1	Q1	Intersil
HIP6007	Standard Buck Controller	SOIC-14	1	U1	Intersil
10kΩ	Resistor, 5%, 0.1 W	0805	1	R7	Various
See Table 2	Resistor, 5%, 0.1 W	0805		R1	Various
See Table 2	Resistor, 5%, 0.1 W	0805	1	R5	Various
1kΩ	Resistor, 5%, 0.1 W	0805	2	R2-R3	Various
See Table 2	Resistor, 1%, 0.1 W	0805	1	R6	Various
576802B00000	Clip-on Heatsink, TO-220		2		AAVID
1514-2	Terminal Post		6	VIN, 12VCC, VOUT, RTN	Keystone
1314353-00	Test Point, Scope Probe		1	VOUT	Tektronics
SPCJ-123-01	Test Point		3	ENABLE, TP1, TP2	Jolo

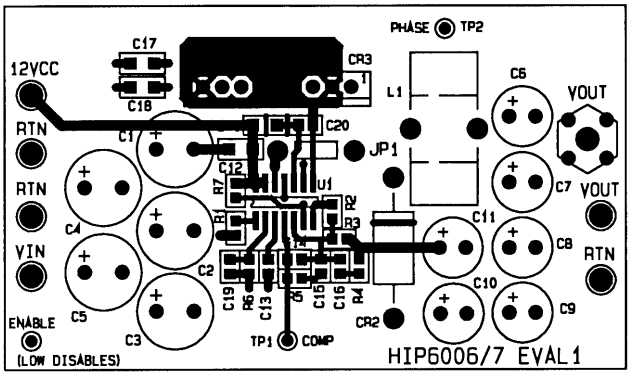
TOP - SILK SCREEN



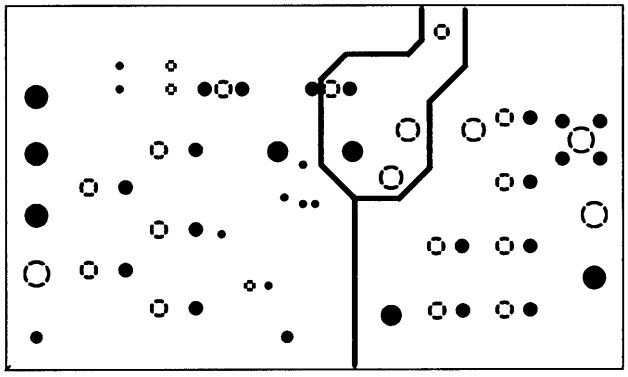
INT GND PLANE



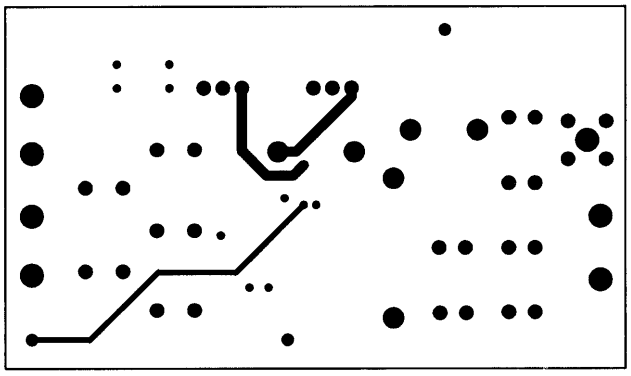
COMPONENT SIDE



INTERNAL ONE



SOLDER SIDE



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